Company Information

Silicon Carbide Laboratory

Dept of Electrical Engineering

University of South Carolina

Area of Expertise

(related to the BAA)

1. Fabrication and characterization of high power SiC PIN diodes.
2. Development of thick epi free of device degrading defects
3. Growth of low defect density bulk 4H-SiC crystals, wafering, and polishing.
4. Wafer-level non-destructive defect identification and mapping.
5. Characterization of electrically active defects in SiC devices undergoing HV testing using EBIC.

Previous Relevant Accomplishments

1. No V_f drift in PIN diodes fabricated by incorporating the p-layer by diffusion (32 μm epi).
2. Demonstrated 80 μm thick SiC epi.
3. Demonstrated 30 μm thick epi on (11-20) plane substrate.
4. No V_f drift in diffused PIN diodes in (11-20) substrate.
5. Demonstrated wafer-level micropipe maps of SiC wafers.
6. Demonstrated visualization of stacking fault development using EBIC.

Contact Information

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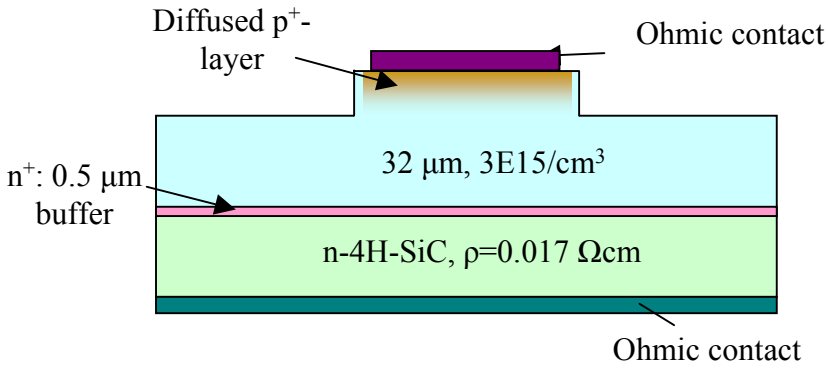
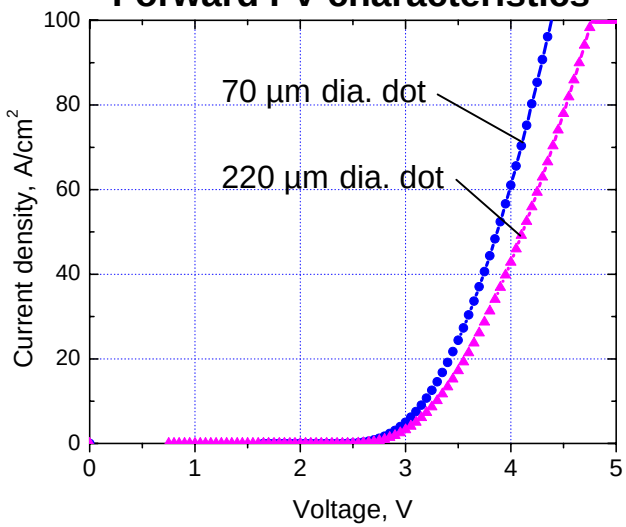
Diffused 4H-SiC PIN diodes with 32 µm thick drift regions formed in (0001) Substrate

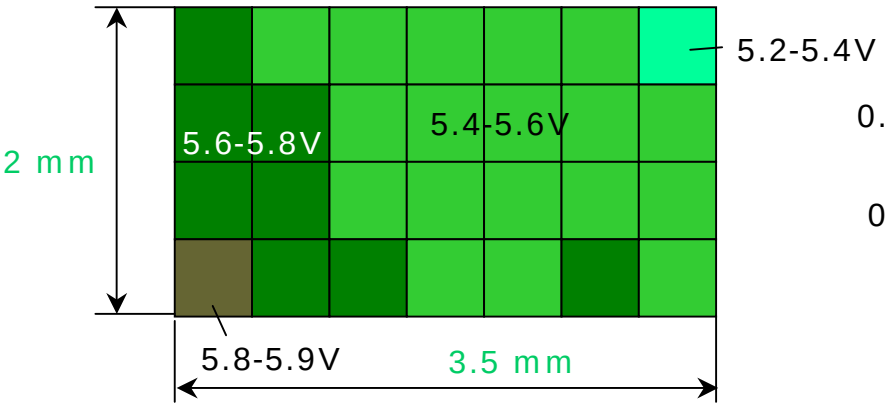
Diode structure



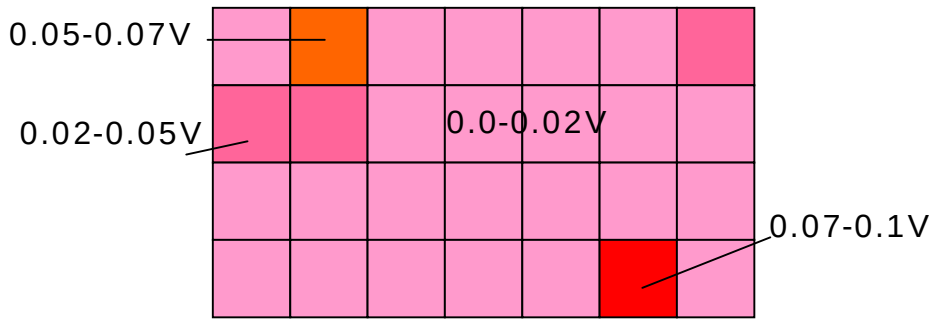
Forward I-V characteristics



Map of Forward Voltage Drop at 200 A/cm^2 for 28 Diodes (220 µm dia.) **before** degradation test



Map of Forward Voltage Drift at 200A/cm^2 for 28 Diodes (220 µm dia.) **after** degradation test



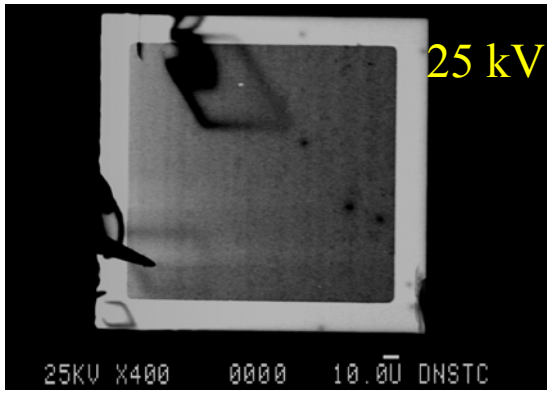
Only one from 28 measured PIN diodes with 32 µm drift regions exhibited maximum forward voltage drift of 0.1 V after high current stress (200 A/cm^2) at room temperature in 1 hour. The 28 PIN diodes were fabricated in an area of 2x3.5 mm.

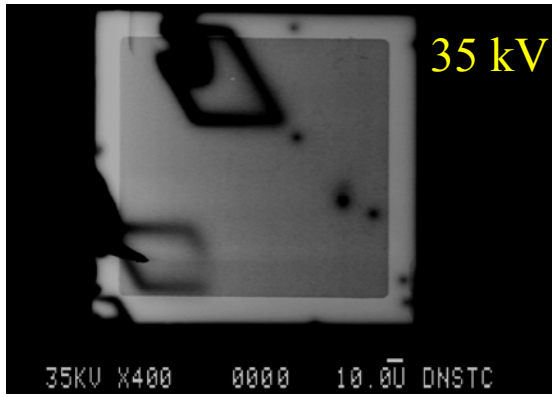
Accomplishment: No degradation demonstrated in diodes formed in substrate with a 32 thick epilayer (test area: 7 mm^2.)

Future: Fabricate and test PIN diodes in substrate with thicker epilayer (>50 µm), investigate reverse characteristics.

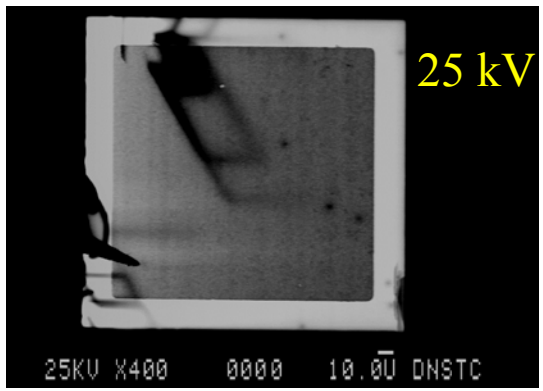
Generation of SFs in 4H-SiC PIN Diode with Epitaxial p^+-Layer. EBIC analysis.

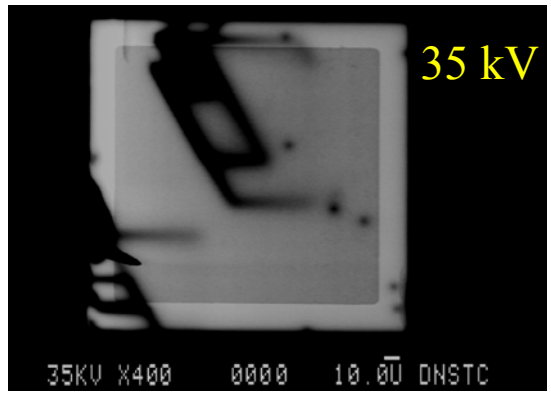
After 60 s of high current stress (200 A/cm^2)





After 90 s of high current stress (200 A/cm^2)

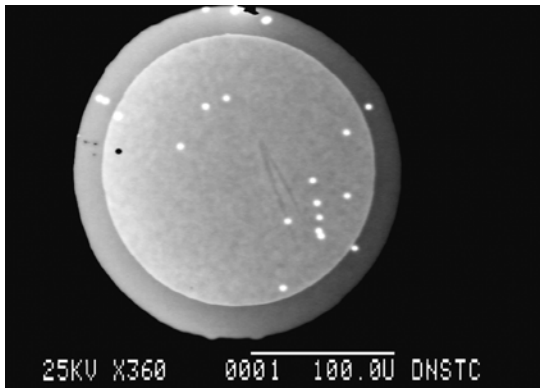




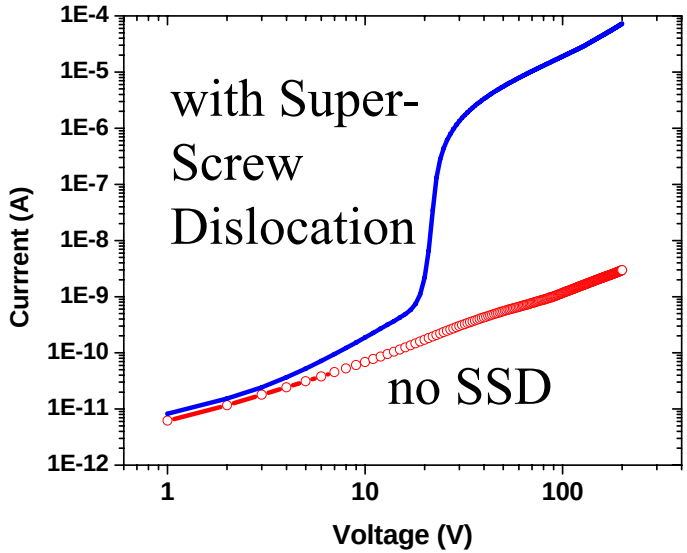
Expansion of SFs occurs from surface to the bulk which was confirmed by varying the energy of primary electrons.

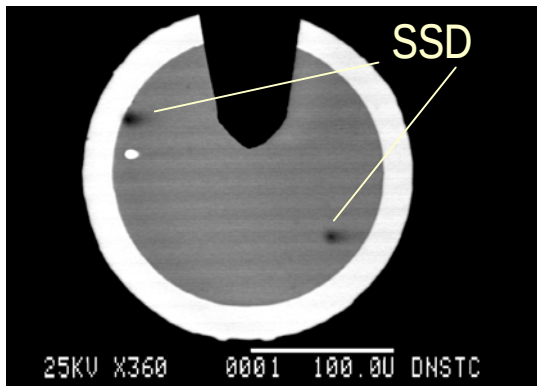
CVD epitaxy of p^+- and n^- layers for this PIN diode was performed in the USC SiC Lab.

Effect of Substrate Defects on Reverse I-V Characteristics

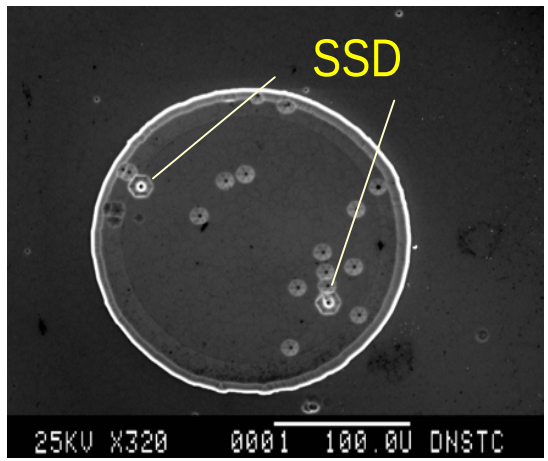


EBIC image at 0V bias





EBIC image at -50V bias

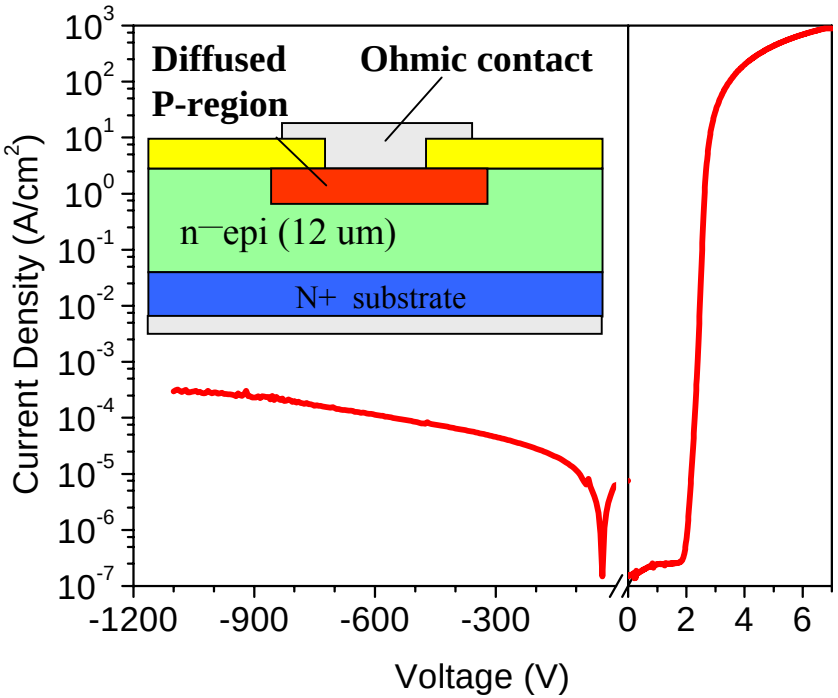


SEM image after etching in KOH

I-V Characteristics of Best SiC Devices Fabricated in USC SiC Lab

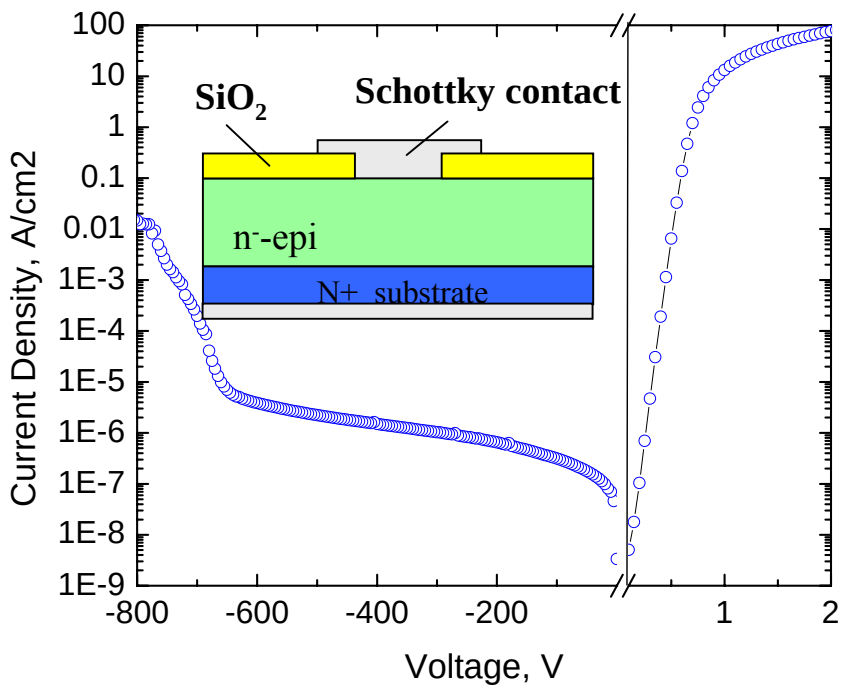
Fabricated on Low Defect Density Substrates

Diffused PIN Diode



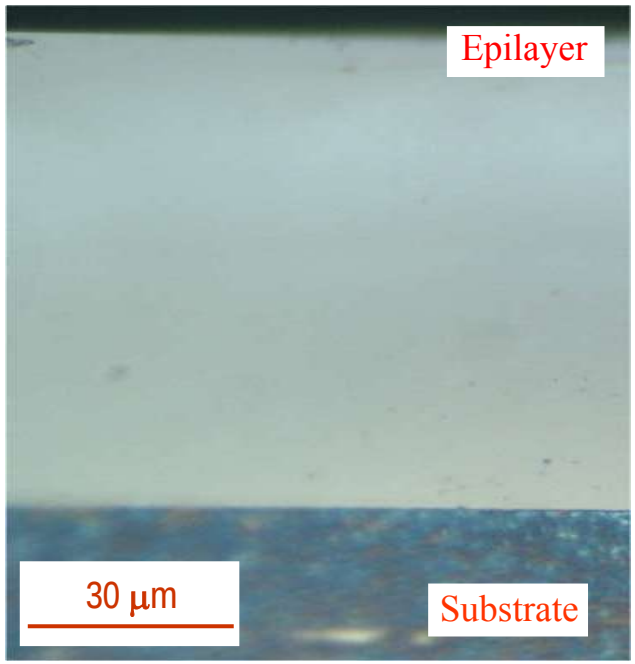
V_{BD}~1100V,
V_f=3.3 V at 100A/cm^2

Schottky Diode

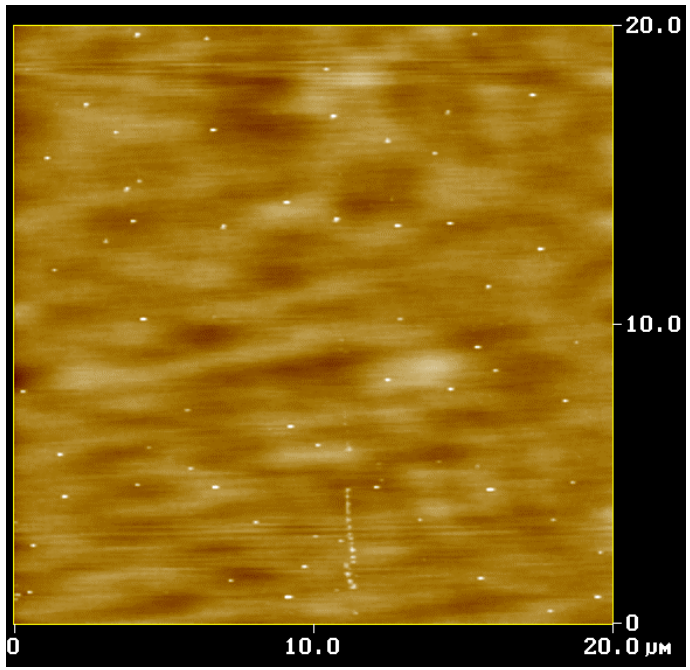


V_{BD}~700V,
V_f=1.9 V at 100A/cm^2

Thick Film Epitaxial Growth on 4H-SiC (0001) Substrate by CVD



Cross-section of (0001) epilayer after anodic oxidation

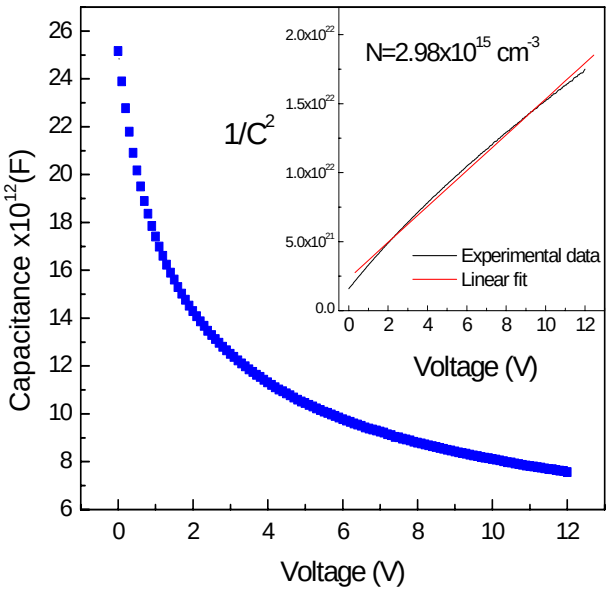


AFM image of the epilayer (RMS roughness is 1.0 nm)

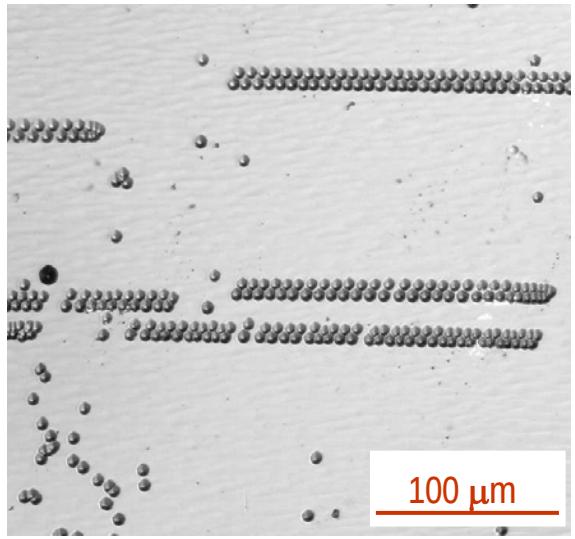
The epilayer with thickness of 80 μm has been grown by 6 hours CVD growth. The epilayer surface morphology is smooth with small undulations seen by AFM. Thick epi-growth capability has been demonstrated in our lab and surface morphology needs to be further improved.

Doping Concentration of Thick Epilayer

Measured by C-V and Structural Defects Decorated by Molten KOH Etching



Capacitance-Voltage (C-V) characteristic of thick epilayer on (0001) face substrate.

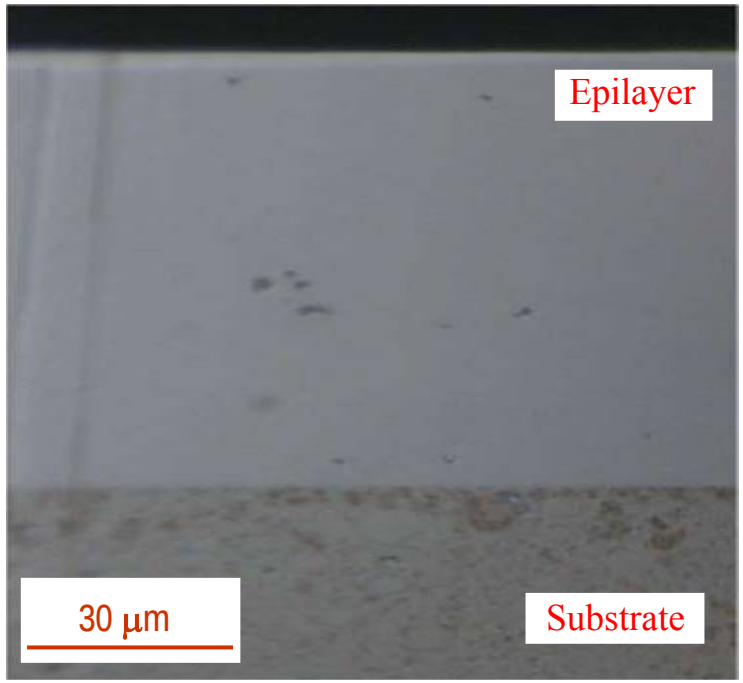


'Pair array' dislocations in epilayer decorated by molten KOH etching

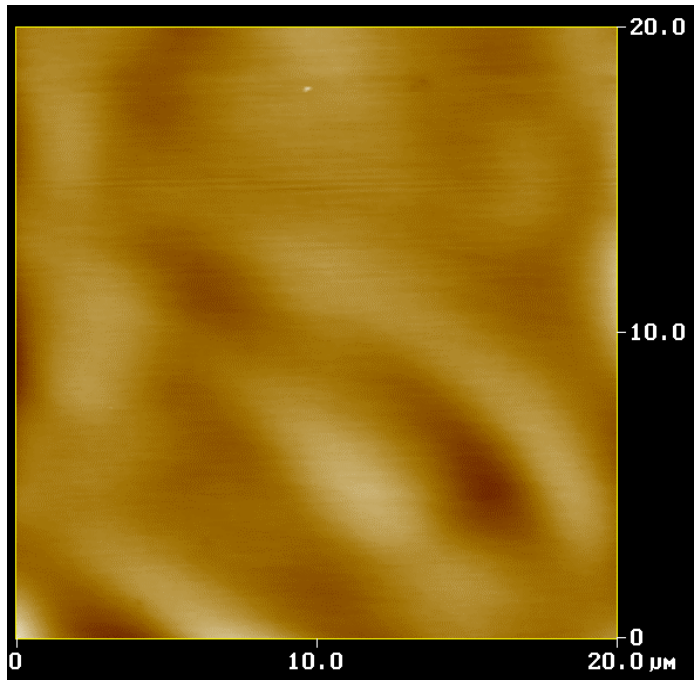
The unintentional doping concentration of (0001) epilayers (80 µm thick) can be controlled to 3×10^{15} cm^{-3} (n-type) by adjusting the C/Si ratio. Further efforts need to be made to reduce the doping concentration $<10^{15}$ cm^{-3} for growing >100 µm ultra thick epilayers.

'Pair array' dislocations start to be generated during growth when the epilayer is around 20 µm thick. These defects degrade the forward performance of bipolar devices. We have a good understanding of the generation mechanism of these defects and an approach to eliminate them.

Thick Film Epitaxial Growth on 4H-SiC (1120) Substrate by CVD



Cross-section of $(1\bar{1}20)$ epilayer decorated by anodic oxidation

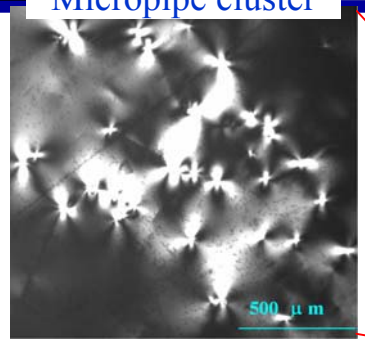


AFM image of the epilayer (RMS roughness is 2 nm). The substrate was polished at USC.

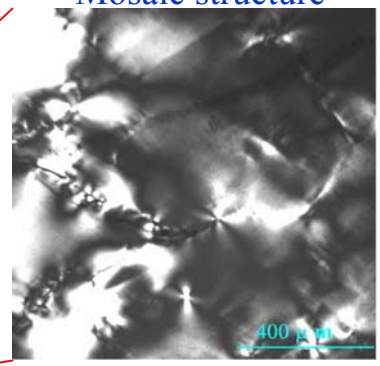
We have succeeded in growing thick epilayer (60 μm) by CVD on *a*-face substrates with good surface quality and doping control: *a*-face substrate is produced by USC.

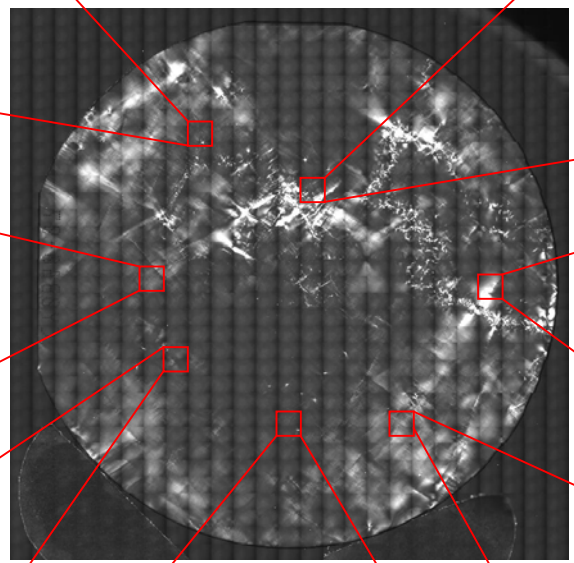
SiC Defect Patterns Delineated by PLM System

Micropipe cluster

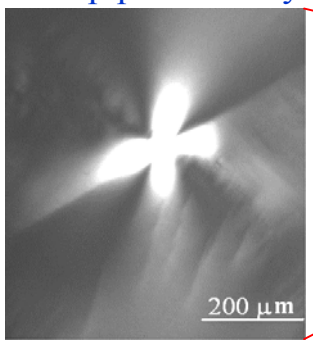


Mosaic structure

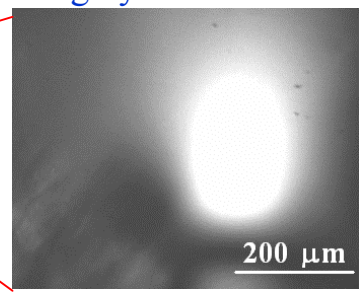




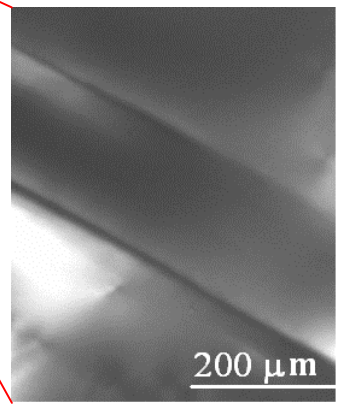
Micropipe: butterfly-shaped



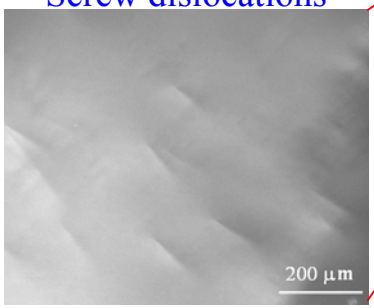
Highly stressed zone



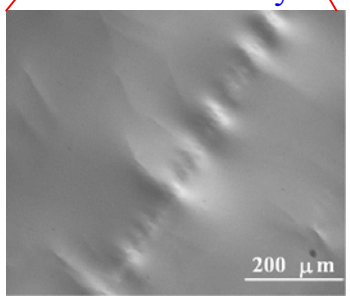
Dislocation or domain wall



Screw dislocations



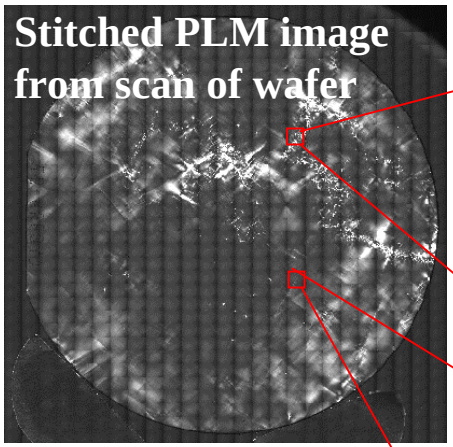
Grain boundary

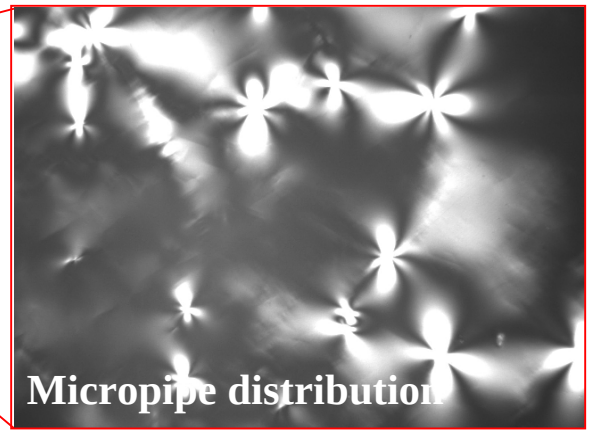


Nondestructive Wafer-scale Defect Mapping

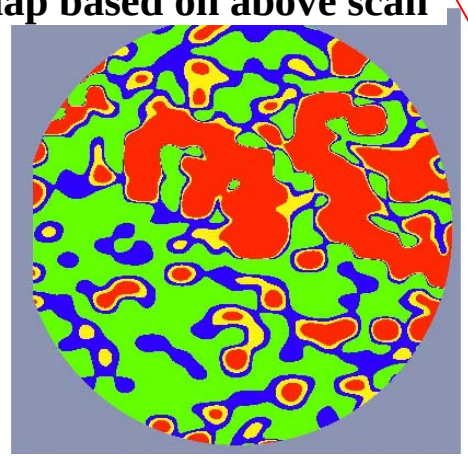
Turn around time: ~15 minutes to fully evaluate a 2-inch wafer.

Pattern Recognition and Defect Analysis

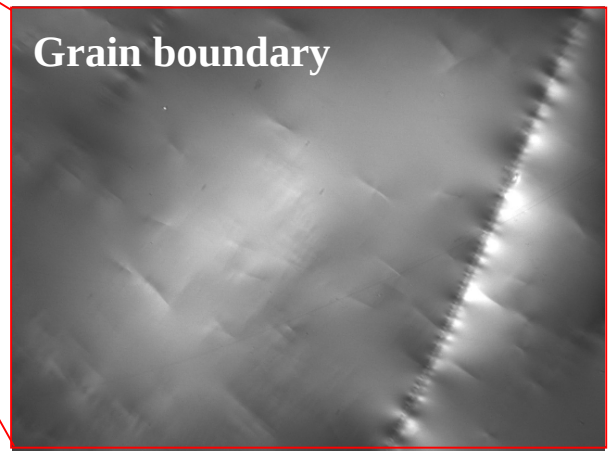




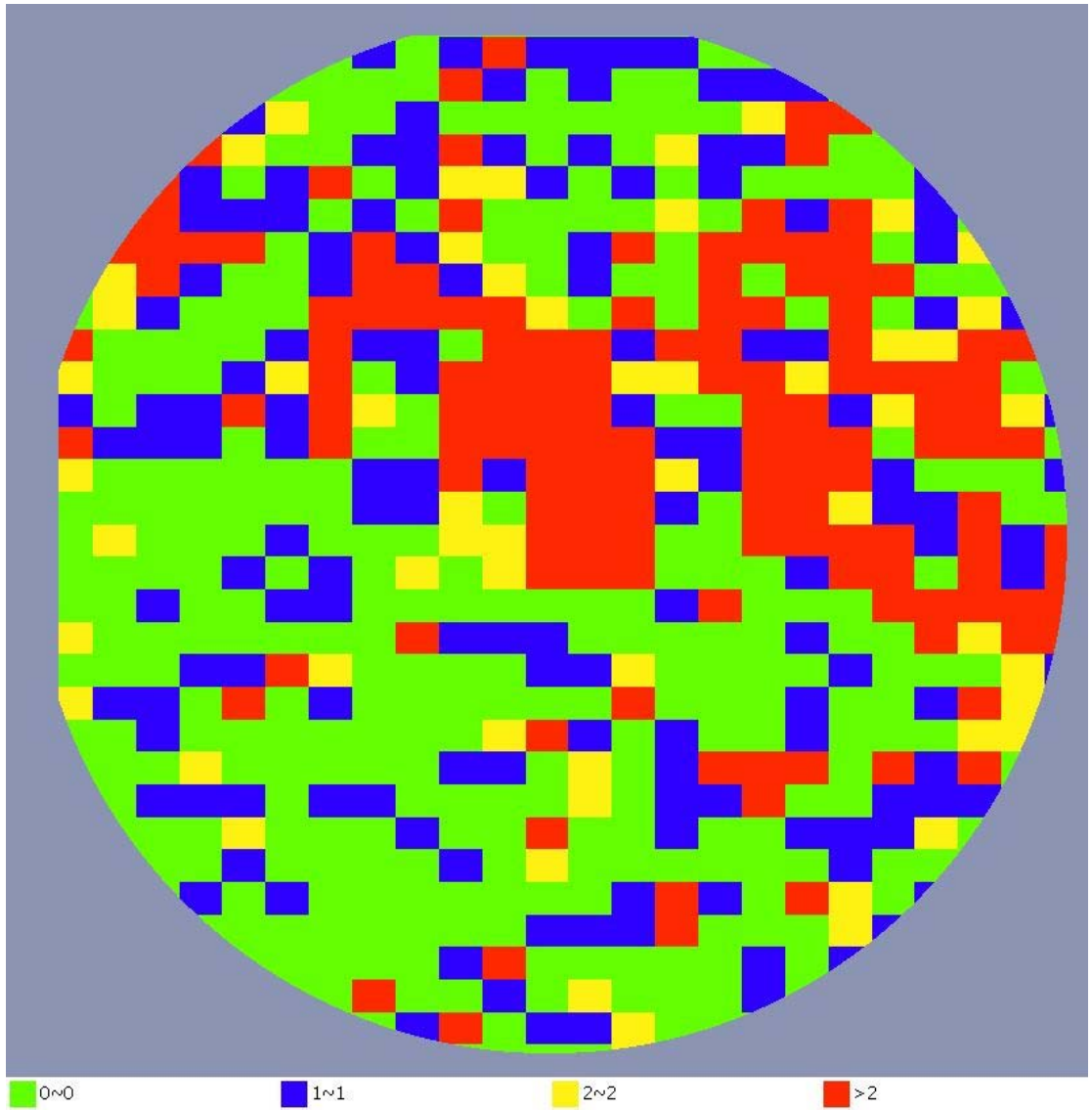
Micropipe distribution map based on above scan



Green – 0; Blue – 1; Yellow – 2; Red > 2



Micropipe Grid Map



Micropipe Contour Map